**1. What is the purpose of schematic capture in Cadence Allegro?**

* a) To define the physical layout of the circuit
* b) To create a graphical representation of the circuit’s components and their connections
* c) To simulate the circuit's behavior
* d) To assign footprints to components

**Answer:** b) To create a graphical representation of the circuit’s components and their connections

**2. Which file format does Cadence Allegro use to save schematic designs?**

* a) .brd
* b) .lib
* c) .dsn
* d) .sch

**Answer:** d) .sch

**3. In Cadence Allegro, which tool is primarily used for schematic capture?**

* a) Layout Editor
* b) Schematic Editor
* c) PCB Editor
* d) Library Manager

**Answer:** b) Schematic Editor

**4. What is a netlist in the context of schematic capture in Cadence Allegro?**

* a) A list of all components used in the schematic
* b) A list of electrical connections between components
* c) A list of all design constraints
* d) A list of all pin names

**Answer:** b) A list of electrical connections between components

**5. What is the primary purpose of placing a symbol in a schematic in Cadence Allegro?**

* a) To define the physical footprint of the component
* b) To define the electrical connections and attributes of the component
* c) To add color to the schematic for clarity
* d) To create the final output for the PCB design

**Answer:** b) To define the electrical connections and attributes of the component

**6. How do you define the attributes of a component (e.g., part number, value) in Cadence Allegro?**

* a) Through the Component Manager
* b) By editing the part's properties in the schematic
* c) By modifying the library symbol
* d) By running a Design Rule Check (DRC)

**Answer:** b) By editing the part's properties in the schematic

**7. What does the "Place" command in Cadence Allegro allow you to do?**

* a) Place components, nets, and other elements in the schematic
* b) Generate a netlist for the design
* c) Validate the schematic for errors
* d) Export the schematic to a PCB layout

**Answer:** a) Place components, nets, and other elements in the schematic

**8. Which of the following actions is required to connect two components in a schematic?**

* a) Use the "Wire" tool
* b) Use the "Route" tool
* c) Manually draw the connection
* d) Use the "Net" tool

**Answer:** a) Use the "Wire" tool

**9. How can you check for electrical errors in your schematic in Cadence Allegro?**

* a) By running a Design Rule Check (DRC)
* b) By reviewing the netlist
* c) By manually inspecting all the pins
* d) By using the Simulation tool

**Answer:** a) By running a Design Rule Check (DRC)

**10. What is the purpose of "Buses" in a schematic capture in Cadence Allegro?**

* a) To group multiple signals or pins into a single connection
* b) To define the power rails for components
* c) To add labels to the schematic
* d) To simulate the circuit behavior

**Answer:** a) To group multiple signals or pins into a single connection

**11. Which of the following is a valid pin type in Cadence Allegro schematic capture?**

* a) Input
* b) Output
* c) Bidirectional
* d) All of the above

**Answer:** d) All of the above

**12. What is the default tool used to modify a component's properties in the schematic editor?**

* a) Properties Tool
* b) Edit Tool
* c) Component Manager
* d) Attribute Editor

**Answer:** d) Attribute Editor

**13. How do you add a new component (part) from the library in Cadence Allegro schematic capture?**

* a) By using the "Library" tool
* b) By using the "Place Part" command
* c) By dragging the component from the component manager
* d) By importing a netlist

**Answer:** b) By using the "Place Part" command

**14. In schematic capture, what is the purpose of the "Hierarchy" feature in Cadence Allegro?**

* a) To create modular designs by grouping components into higher-level blocks
* b) To define the physical footprint of a component
* c) To simulate the electrical performance of the circuit
* d) To create different versions of the design

**Answer:** a) To create modular designs by grouping components into higher-level blocks

**15. Which of the following would you use to ensure that your schematic is connected properly?**

* a) Run Electrical Rule Check (ERC)
* b) Use the "Wire" tool
* c) Manually check all connections
* d) Run the Design Rule Check (DRC)

**Answer:** a) Run Electrical Rule Check (ERC)

**16. What is the benefit of using "Aliases" for pins in Cadence Allegro?**

* a) To assign alternative names to components or nets for clarity
* b) To simulate the pin's electrical behavior
* c) To improve the design rule checks
* d) To define different pin orientations

**Answer:** a) To assign alternative names to components or nets for clarity

**17. How do you import an existing netlist into a schematic in Cadence Allegro?**

* a) Through the "File" menu and choosing "Import Netlist"
* b) By using the "Import Part" tool
* c) By pasting the netlist manually
* d) Netlists cannot be imported into Allegro directly

**Answer:** a) Through the "File" menu and choosing "Import Netlist"

**18. What is the "Annotation" tool used for in Cadence Allegro schematic capture?**

* a) To add comments or labels to the schematic for documentation purposes
* b) To assign a unique part number to a component
* c) To assign values to components
* d) To group components together

**Answer:** a) To add comments or labels to the schematic for documentation purposes

**19. What is the purpose of running the "ERC" (Electrical Rule Check) in Cadence Allegro?**

* a) To check the schematic for electrical connectivity errors
* b) To check the schematic for design rule violations
* c) To optimize the layout of the components
* d) To simulate the schematic

**Answer:** a) To check the schematic for electrical connectivity errors

**20. In Cadence Allegro, how do you ensure that a part has a corresponding footprint in the PCB layout?**

* a) By linking the part in the schematic to its footprint in the library
* b) By manually placing the footprint after the schematic is complete
* c) By running the Design Rule Check (DRC)
* d) By setting the part’s attributes to include a footprint name

**Answer:** a) By linking the part in the schematic to its footprint in the library